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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,058	09/08/2003	Bruce L. Troutman	ZILG.244US1	5500

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EXAMINER	
CHOI, WOO H	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,058	TROUTMAN ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 25-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12,25-32 and 34-40* is/are rejected.

7)☐ Claim(s) *33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Newly added claims 38 – 40 are labeled as "(Original)". These are new claims and should be labeled as such.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 34 – 37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The newly added claims require that "all of the members of the instruction set" be stored contiguously. This would mean that if a microprocessor's instruction set consists of N different instructions that the microprocessor can recognize and execute, all N instructions must be stored in the claimed memory. The Examiner notes that "an instruction set" for a microprocessor is a term of art that refers to the set of machine instructions that a given processor recognizes and can execute. It is not an arbitrary collection of executable instructions, i.e. a set of instructions, such as an "executable program" that a programmer creates. An instruction set is created by the designer of the microprocessor and "all of the members of the instruction set" refers to the entire

set of instructions recognized by the microprocessor. The specification does not disclose storing of "all of the members of the instruction set" in the claimed memory.

4. The examiner notes that the original claim 25 also recites a similar limitation requiring "programming the instruction set into the memory". However, the Examiner interpreted this limitation in light of the specification and the limitation was not construed to require that the entire set be programmed, as it seemed pretty clear to the Examiner that the claimed memory is for storing a set of instructions, not an entire instruction set. Instead, the limitation was interpreted as a "set of instructions of the instruction set" in the previous action. However, the Examiner **strongly recommends** that this limitation be amended to state "programming a set of instructions of the instruction set" or other similar limitations that avoid storing of the entire instruction set. Such an amendment would avoid a potential scope of enablement issue since the interpretation that requires that the entire instruction set be programmed is also reasonable and valid. Even if allowed, Applicant may end up with an unintended invention that may not be of much use if the above concern is not addressed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 9, 11, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kojima *et al.* (US Patent No. 5,880,981, hereinafter "Kojima").

7. With respect to claim 8, 11, and 12, Kojima discloses a microprocessor (figure 1), comprising:

a central processing unit (30) with an instruction set including three-byte instructions (col. 4, lines 27);

a one time programmable memory for storing the instructions (5. col. 4, lines 23 – 24), wherein the instructions are stored contiguously (5 is a program memory that stores 24 bit instruction words in an array of 24 bit by 1K contiguous block as shown in figure 1); and

a memory interface that comprises a three-byte wide bus (figure 1, 9) for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said instructions are supplied simultaneously in a single fetch operation (col. 4, lines 55 – 56).

8. Claims 10, 25, 27, 29 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Picket *et al.* (US Patent No. 6,101,595, hereinafter "Pickett").

9. With respect to claim 10, Pickett discloses a microprocessor 9figure 1), comprising:

a central processing unit with an instruction set including one-byte, two-byte, and three-byte instructions (figure 5, IN1, IN3, IN2);

a memory for storing the instructions (figure 3, 112) , wherein the instructions are stored contiguously (figure 5, IN2 and IN3 are contiguous) ; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said instructions are supplied simultaneously in a single fetch operation (col. 7, lines 11 – 13).

10. With respect to claim 25, Pickett discloses a method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte (figure 5, IN2, N=3) instructions, a memory for storing the instructions (figure 3, 112), and a memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M-byte wide columns (figure 3, M = 32, see col. 7, lines 2 – 4), wherein M is an integer greater than one and wherein N and M are relatively prime (3 and 32 are relatively prime);

programming the instruction set into the memory, wherein the instructions are stored contiguously in the memory (figure 5, IN2 and IN3 are contiguous); and

operating the interface whereby each of the instructions can be supplied from the memory to the central processing unit in a single fetch operation (col. 7, lines 11 – 13).

11. With respect to claim 27, said instruction set further includes two byte instructions and one byte instructions (figure 5).

12. With respect to claims 29 and 39, the memory is an embedded memory of the microprocessor (instruction cache 16 is an integral part of the microprocessor).

13. Claims 9, 25, 26, 29 – 32, 39, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (US Patent No. 5,765,212).

14. With respect to claims 9, 25 and 26, 31, 32 Yamada discloses a method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte (col. 4, lines 46 – 50, N=3) instructions, a memory for storing the instructions (figure 1, ROMs 100 – 103), and a memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M-byte wide columns (figure 1, M = 4), wherein M is an integer greater than one and wherein N and M are relatively prime (3 and 4 are relatively prime);

programming the instruction set into the memory, wherein the instructions are stored contiguously in the memory (col. 2, lines 1 – 8, and col. 6, lines 29 – 39 and lines 60 – 64, Yamada's invention allows fetching of 3 bytes of unaligned instructions, i.e. starting from any byte column, in a single fetch cycle, so space between instructions that may be need for aligned instructions is not needed); and

operating the interface whereby each of the instructions can be supplied from the memory to the central processing unit in a single fetch operation (col. 6, lines 29 – 39 and lines 60 – 64).

15. With respect to claims 29, 30, 39, and 40, the memory is an embedded ROM (col. 1, lines 14 – 17, 34 – 37).

16. Claims 28 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki *et al.* (US Patent No. 5,809,306, hereinafter "Suzuki").

Suzuki discloses a method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte (figure 16 A, N=2, see also col. 27 instructions 3 and 5, they appear to be one byte instructions as the addresses of the instructions that follow are incremented by 1) instructions, a memory for storing the instructions (figure 13, 130), and a memory interface for supplying the instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M-byte wide columns (col. 29, line 26, 24 bit data bus implies 3-byte columns), wherein M is an integer greater than one and wherein N and M are relatively prime (2 and 3 are relatively prime);

programming the instruction set into the memory, wherein the instructions are stored contiguously in the memory (col. 31, assembly code segments show contiguous storage of instructions); and

operating the interface whereby each of the instructions can be supplied from the memory to the central processing unit in a single fetch operation (by definition a single instruction can be fetched in a single instruction fetch operation).

Allowable Subject Matter

17. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

18. Applicant's arguments with respect to claims 9 – 12 and claims rejected with Baji reference have been considered but are moot in view of the new ground(s) of rejection.

19. Applicant's argument regarding the Pickett reference is not persuasive. Pickett clearly shows storing instructions contiguously as discussed above. The claim does not require that all instructions be stored contiguously without any gap as argued. It merely requires that the instructions be stored contiguously. If claim 25 requires storing of the entire instruction set, as Applicant seems to be arguing, instead of a set of instruction as explained above, rejections based on the Pickett reference will be withdrawn in the next Office Action if Applicant makes the same argument.

In addition to the contiguous storage of at least two instructions shown in figure 5, Pickett discloses that instructions are stored contiguously in at least one other way. Pickett's memory is an instruction cache, which is a physical memory that stores only instructions. The cache is organized as rows of 32-byte columns, with each row representing a 32-byte cache line. The

first row of instructions is contiguously stored with the second row, the second row with the first and the third row, etc...

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 21, 2005

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